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EXAMINER	
PATEL, GAUTAM	

ART UNIT	PAPER NUMBER
2655	27

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/266,869	TANIGUCHI ET AL.	
	Examiner	Art Unit	
	Gautam R. Patel	2655	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16-18,25,26 and 28-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16-18, 25-26 and 28-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-14, 16-18, 25, 26 and 28-36 are pending for the examination. Claims 35-36 are newly presented.

RCE STATUS

2. The request filed on 10-9-01 for Request for continued Examination (RCE) under 37 CFR 1.114 based on parent Application is acceptable and a RCE has been established. An action on the RCE follows.

NOTES & REMARKS

3. Applicant's arguments regarding rejection of claims 1-13, 24, 26-30 and 32-34 under 35 U.S.C. § 112 first paragraph have been fully considered and rejection of old claims 1-13, 24-34 under 35 U.S.C. 112 first and second paragraph has been **withdrawn**. However claims 25, 28 and 30 has NOT been amended to remove 112 first rejection as was given previously.

4. Applicants amendment has overcome new matter issue and objection is **withdrawn**.

Claim Rejections - 35 U.S.C. § 112

5. The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 25, 28, 30 and 32 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Page 7, 18 and 25 simply states "that a pseudo instruction is defined to be handled in the same manner as a (NOP) instruction by the execution unit 12". The specification does **not** disclose at all that a pseudo instruction is handled as NOP instruction when the pseudo instruction is **detected**.

Claims 28 , 30 and 32 has same problem as claim 25.

6. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 25, 28, 30, and 32 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is confusing as to how the pseudo instruction is handled as a no-operation instruction when pseudo instruction is detected, or this detection is related to handling of pseudo instruction.

Claim Rejections - 35 U.S.C. § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 6-8, 16-18 and 34-35 are rejected under 35 U.S.C. § 102(b) as being anticipated by Cocke et al., US. patent 3,577,189 (hereafter Cocke).

As to claim 1, Cocke discloses the invention as claimed [see Figs. 1-7A; especially fig. 5] including detecting pseudo instruction and arranging it before one instruction reading a program, reading data. Storing instruction or data and executing data, comprising the steps of:

reading the program from the memory [storage system; col. 5, lines 21-23], wherein the program includes a pseudo instruction [fig. 5, instruction labeled as "BRANCH", instruction after Opa3] and at least one branch instruction [fig. 5, "EXIT" instruction], or at least one call instruction, the

pseudo instruction being arranged before the branch instruction [BRANCH instruction comes before "EXIT" instruction] [col. 10, line 67 to col. 11, line 5] or the call instruction and including an address for a branch destination instruction or a call instruction [col. 4, line 49 to col. 5, line 2]; [col. 1, line 73 to col. 2, line 45];

detecting the pseudo instruction with a first unit [fig. 1A, unit 8] [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5];

reading the instruction from the main memory in accordance with the address for the branch destination instruction or the call destination instruction [col. 5, lines 20-40] with the first unit when pseudo instruction is detected [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5];

storing the instruction in a buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]; and

executing the stored instruction with a second unit [execution unit] [col. 1, line 73 to col. 2, line 45]. (NOTE: Execution unit is inherently present in any computer system and is inherently separate from predecode unit.)

NOTE: As it has been pointed out by the Examiner that "prepare to branch" and related concepts are well known in the art for a very long time. The vocabulary is slightly different in old patents. Cocke's so called **"BRANCH instruction"** works as **a pseudo instruction** and Cocke's so called **"EXIT instruction"** is actually **a branch instruction** in today's vocabulary. Also Cocke "storage system" is his "memory".

8. As to claim 2, Cocke discloses:

a pseudo instruction [branch instruction] detection unit [Fig. 1A, unit 8] connected with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit in parallel [see lines 6 and 10 in fig. 1A] with the buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

9. As to claim 6, Cocke discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address with the first unit after the transfer of the at least one instruction to the first buffer has been identified [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

10. As to claim 7, Cocke discloses:

Identifying that the corresponding instruction is stored in the second buffer in accordance with the at least one instruction address with the first unit when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction is not stored in the second buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

11. As to claim 8, Cocke discloses:

a buffer [fig. 1A, unit 2], connected to a memory ["storage system"; col. 5, lines 21-23], for storing a program read from the memory, wherein the program includes a pseudo instruction [fig. 5, instruction labeled as "BRANCH", instruction after Opa3], and at least one branch instruction [fig. 5, OPa4], or at least one call instruction, the pseudo instruction being arranged before the branch instruction or the call instruction and including an address for a branch destination instruction or a call destination instruction [col. 1, line 73 to col. 2, line 75 and col. 3, lines 36-54];

a first unit [fig. 1A, units 4 and 8] including,

a pseudo instruction detection unit [fig. 1A, unit 8], connected to the memory, for detecting the pseudo instruction included in the program read from the memory;

an address control unit [inherently present, since Cocke is calculating addresses], connected to the memory and the pseudo instruction detection unit, for reading the instruction from the memory in accordance with the address for a branch

destination instruction or a call destination instruction when the pseudo instruction is detected and storing the instruction in the buffer [col. 1, line 73 to col. 2, line 45]; and

a second unit [execution unit] connected to the buffer, for executing the instruction [col. 1, line 73 to col. 2, line 45] stored in the buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]. NOTE: Since Cocke is executing instructions execution unit is inherently present.

12. As to claim 16, it is rejected for the same reasons set forth in the rejection of claim 1 and 8, supra.

As to the added limitation of

a bus [fig. 1, unit 6] interconnecting the prefetch buffer [fig. 1, unit 8] and the memory [storage system; col. 5, lines 21-23].

A holding circuit [fig. 1A, unit 2].

13. As to claim 17, Cocke discloses:

the pseudo instruction detection unit further comprises:

a pseudo instruction detection circuit that receives at least a part of each of the instructions being transferred from the memory to the prefetch buffer, detects an opcode of a pseudo instruction therefrom, and generates a detection signal; and

a shift register [fig. 1A, unit 2 and ROW 0, 1, 2 etc works as shift register as they are pushing instructions down from one level to next; see col. 10, lines 67-75] connected to the pseudo instruction detection circuit and receiving the detection signal, and generating a hold circuit enable signal, wherein when the hold circuit enable signal is active, the holding circuit stores the pseudo instruction operands being transferred on the bus [col. 4, lines 49-75].

14. As to claim 18, Cocke discloses:

an additional information holding circuit that stores a first operand [fig. 1A, ROW 0, block "I"] of the pseudo instruction;

an upper address holding circuit that stores a second operand [fig. 1A, ROW 0, block "J"] of the pseudo instruction; and

a lower address holding circuit that stores a third operand [fig. 1A, ROW 0, block "K"] of the pseudo instruction, wherein the second and third operands comprise a memory address [col. 4, lines 49-75 especially 64-68].

15. As to claim 34 it is rejected for the same reasons set forth in the rejection of claim 1, supra.

16. As to claim 35, Cocke discloses:

the stored instruction is executed in a next cycle after the branch instruction or the call instruction [col. 4, line 49 to col. 5, line 2]; [col. 1, line 73 to col. 2, line 45];

Claim Rejections - 35 U.S.C. § 103

17. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

18. Claims 3-5, 9-14, 26, 29, 31 and 33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cocke as applied to claims 1-2, 6-8, 16-18, 30, 32 and 34-35 above.

As to claim 3 Cocke discloses:

. the buffer includes first [fig. 1A, unit 2, sub-unit ROW N] and second [fig. 1A, unit 2, sub-unit ROW 0] buffers connected, and the method further comprising a step of storing, the instruction read from the memory in the first buffer and storing the instruction included in the detected pseudo instruction in the second buffer [col. 5, lines 17-48 and col. 7, lines 38-50];

Cocke does not teach that the buffers are connected in parallel to the main memory [storage system]. However it would have been obvious to a person of ordinary skill at the time of the invention to have placed the buffer and detection unit in parallel and put them into the system of Cocke because doing so would make design more faster. As shown in "In re Japikse **86 USPQ 70 (CCPA 1950)**", to rearrange parts for different storage method is generally not given patentable weight or would have been obvious improvements.

19. As to claim 4, Cocke discloses:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with first unit when the pseudo instruction is detected [fig. 5 and col. 10, line 56 to col. 11, line 34]; and

prefetching the instruction from the memory [col. 3, lines 36-54] in accordance with the at least one instruction address with the first unit after the transfer of the at least one instruction to the first buffer has been identified [col. 1, line 73 to col. 2, line 75].

20. As to claim 5, Cocke discloses:

Identifying that the corresponding instruction is stored in the second buffer in accordance with the at least one instruction address when the pseudo instruction is detected wherein the prefetch step is executed when the corresponding instruction is not stored in the second buffer [col. 1, line 73 to col. 2, line 75 and col. 3, lines 36-54].

21. As to claim 9, it is rejected for the same reasons set forth in the rejection of claim 3, supra.

22. As to claim 10, Cocke discloses:

the address control unit identifies that the corresponding instruction is stored in the second buffer in accordance with the at least one instruction address when the pseudo instruction is detected and permits storage of the instruction in the second buffer when the corresponding instruction is not stored in the second buffer [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5].

23. As to claim 11, it is rejected for the same reasons set forth in the rejection of claim 2, supra.

24. As to claim 12, it is rejected for the same reasons set forth in the rejection of claim 10, supra.

25. As to claim 13, it is rejected for the same reasons set forth in the rejection of claim 11, supra.

26. As to claim 14, Cocke discloses:

a detection circuit [Fig. 1A, unit 8], connected to the memory ["storage system"; col. 5, lines 21-23], for receiving the pseudo instruction read from the memory and detecting the opcode included in the pseudo instruction [col. 5, lines 17-48 and col. 10, line 67 to col. 11, line 5]; as to the rest of the claim

Cocke discloses all of te above elements including detection circuit. Cocke does not disclose a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for validating the opcode detection operation during an operand transfer period. "Official Notice" is taken that both the concept and the advantages of providing a detection timing circuit which can calculate transfer period based on the instruction length and number of operands are well known. It would have been obvious to provide a timing circuit to

Cocke' system as this circuit is known to provide the system with a timing estimate and send valid operand into the system. These concepts are well known in the art and do not constitute a patentably distinct limitation, per se [M.P.E.P. 2144.03].

27. As to claims 26 and 29, Cocke discloses all of the above elements including second unit. Cocke does not specifically disclose that the second unit [execution unit] ignoring an address for the pseudo instruction when receiving the address for the at least one instruction or the address for the data [i.e. skips the pseudo instruction and executes the prefetched instruction]. However one of ordinary skill in the art at the time invention would have realized that computer time and resources are at premium and it would be unwise, and useless, to execute an instruction that is not producing any results in the execution unit. One would have been motivated to make system faster by not performing unnecessary tasks.

Therefore it would have been obvious to have skipped the execution of the pseudo instruction in the system of Cocke because it would have saved time and resources during execution by not executing unnecessary instruction.

28. As to claims 31 and 33, they are rejected for the same reasons set forth in the rejection of claim 30, supra. As to the added limitations:

Cocke does not disclose the added limitation of second unit [execution unit] skips the pseudo instruction and executes the prefetched instruction. However one of ordinary skill in the art at the time invention would have realized that computer time and resources are at premium and it would be unwise and useless to execute an instruction that is not producing any results in the execution unit. One would have been motivated to make system faster by not performing unnecessary tasks thus saving computer time.

Therefore it would have been obvious to have skipped the execution of the pseudo instruction in the system of Cocke because it would have saved time and resources during execution by not executing unnecessary instruction.

Claim Rejections - 35 U.S.C. § 103

29. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

30. Claim 36 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants admitted prior art (AAPA) (specification page 1-2) in view of Hoskins, US. patent 5,872,978 (hereafter Hoskins).

As to claim 1, AAPA Hoskins discloses the invention as claimed [see Figs. 1], including reading program from memory and detecting pseudo instruction comprising: a method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction, the pseudo instruction being arranged before the at least one instruction and indicating that the at least one instruction or data follows the pseudo instruction, at least one instruction address of or data address being part of the pseudo instruction [see spec. Page 1, line 22 to page. 2, line, 7] the method comprising the steps of:

reading the program from the memory [spec. Page 1, line 22 to page. 2, line, 7];

prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address; and

storing the prefetched instruction or data in a buffer [spec. Page 1, line 22 to page. 2, line, 7].

regarding claim 1 , AAPA teaches prefetching of instruction or data from a memory AAPA also teaches detecting a branch instruction prior to execution of the branch instruction. AAPA proposes a hardware solution for the detection of branch. Hoskins proposes a software solution for detecting a branch. One skilled in the art would have clearly recognized that the software reduces the cost of extra hardware necessary to implement the detection scheme. One of ordinary skill in the art at the time of invention would have been motivated to implement Hoskins' branch detection scheme with the help of the pseudo-instruction [col. 2, lines 4-21] in the system of AAPA, because it would have reduced the cost of system implementation.

31. A search based on the best understanding of the claims has been made to find the most pertinent art, but no statement about invention will be appropriate at this time regarding the allowableness of claims 25, 28 , 30 & 32 and no art rejection will be made in this office action regarding the claims 25, 28 , 30 and 32 due to the speculation required to interpret the claims because of their indefiniteness under 35 U.S.C. 112, 1st and 2nd paragraphs as noted above (see In re Steele, 134 USPQ 292).

Cocke and Hoskins were cited as prior art references previously.

32. Applicant's arguments filed on 5-9-03 (Paper # 19) have been fully considered but they are not deemed to be persuasive for the following reasons.

33. In the REMARKS, the Applicant argues as follows:

A) That: "Cocke teaches the occurrence of an exit instruction after the presence of a branch instruction. By contrast, the pseudo instruction as set forth in the claimed invention occurs prior to the presence of the branch instruction (or call instruction). Additionally, neither the branch instruction nor the exit instruction disclosed in Cocke

corresponds to the pseudo instruction as set forth in the claimed invention." [page 15, para. 4; REMARKS].

FIRST: Please read the explanation of OLD and NEW terminology that was given several times before under claim 1 regarding what is branch instruction what is pseudo instruction what exit instruction and how they relate to each other.

SECOND: It is not important what words are used for each instruction on old days and now days. It is more important as what these instructions are DOING. It is their **function** which defines what they are NOT what they are called.

Contact Information

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Doris To can be reached on (703) 305-4827.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

Gautam R. Patel
Primary Examiner
Group Art Unit 2655

March 25, 2004